4.10 Bus Interfaces

There are six buses supported by IRIS systems - VME, GIO, EISA, PCI, IBUS and XIO bus. The VME, GIO, EISA and PCI buses are buses that developers can create boards for. The IBUS and XIO buses are proprietary buses developed by Silicon Graphics and not generally available for developers to design to.

Most of the early systems supported VME where add-in cards could be either 6U or 9U sized. 6U sized cards were added using an extender board. Although the card slots for Twin Tower, Single Tower, Deskside and Rack systems are all 9U sized, not all of these slots are configured as VME slots. This is covered in more detail in the section on backplanes starting on page 4-133. The Personal IRIS supported one 6U VME card.

Starting with the Indigo, the GIO (Graphics I/O) bus became the bus for expansion. There are three variations of the GIO bus. Two are physically identical, differing only in the bus protocol (GIO32 and GIO32-bis). The board size for these two is roughly 3" by 6". The third, GIO64, is a much larger board and, as can be noted from the name, is 64 bits wide instead of 32 bits wide. Boards for this bus are roughly the same size as EISA boards since both GIO64 boards and EISA boards live in the same backplane. The outline of the board does differ from a standard EISA board however. A more detailed description of the GIO bus protocols, electrical requirements and pinouts is documented in the GIO Bus Specification. This document is available (under non-disclosure) from the Developer Program.

The IBUS is the connection that is available on the IO4 board. Silicon Graphics makes several "mezzanine" boards available that use this interface. An example is the Audio/Serial Option (ASO) board (see Section 4.1.4 and Table 4-51). Due to the complexity and cost of design this bus is not generally available for developers for design purposes.

The EISA bus is the industry standard bus as used by the PC community. It's data paths are 32 bits wide. The Indigo^2 is the only chassis that supports the EISA bus. With the introduction of the Indigo^2 systems with IMPACT graphics, the number of EISA and GIO connectors changed due to additional components and connectors on the backplane.

The newer series of systems (O2, OCTANE, Origin200, Origin2000 & Onyx2) include PCI bus capability. The PCI bus supports both 32 and 64 bit PCI cards. The "PCI Developer Guide", available from the Developer Program, documents the PCI bus and the architectures where it can be found.

The XIO bus is also used in the newer series of systems (with the exception of the O2 and Origin200). This is a proprietary bus of very high bandwidth. Some of the subsystems of the OCTANE, Origin2000 and Onyx2 are implemented as XIO modules. A good example is the graphics for OCTANE, the Server Base I/O module for the Origin2000 and the Graphics Base I/O module for the Onyx2. Again, due to the complexity and cost of design this bus is not generally available for developers for design purposes.

A simple comparison of bus bandwidths is shown in Table 4-62.

Table 4-62 Bus Bandwidths

Bus	Bus WIdth	Maximum Bandwidth
VME	32 bits	26 - 28 MB/sec
GIO32 or GIO32-bis	32 bits	100 MB/sec
GIO64 (Indigo^2)	64 bits	200 MB./sec
EISA (Indigo^2)	32 bits	18 - 21 MB/sec
PCI	32 bits 64 bits	100 MB/sec 200 MB/sec
IBUS	64	280 MB/sec
XIO	16	800 MB/sec

Table 4-63 shows which busses are supported by IRIS chassis. Numbers in the table indicate how many boards or slots are available but not necessarily the total number of slots contained in the chassis. For VME systems many of the 9U slots are used by CPU or graphics cards that do not have a VME pinout (or in some cases VME-like connectors).

The table also does not address the number of boards or slots available in large multi-rack systems such as the Origin2000 and Onyx2. The numbers quoted in the table reflect the number of boards or slots in a single rack module.

Specific notes related to Table 4-63 are:

1. These slots are also used by the CPU, disk controllers, ethernet and any memory boards.
2. Predator Servers have 2 VME busses. Bus A has 6 slots, Bus B has 5 slots.
3. The Onyx system may add either an expansion VME card cage providing 20 additional VME64 slots, or a graphics expansion card cage providing 6 additional VME64 slots (as well as additional graphics slots).
4. The Challenge XL system may add an expansion VME card cage providing 20 additional VME64 slots.
5. GIO64 and EISA boards in an Indigo^2 share 4 *physical* slots.
6. VME 64 slots on Eveready and Terminator chassis do not support VSB pins.
7. The backplane for the IMPACT has four physical GIO64 connections, but there are only two logical GIO64 connections.
8. The PCI Card Cage is an option on the OCTANE, Origin2000 and Onyx2 systems

Table 4-63 Bus Interfaces on IRIS Systems

Chassis	Model/ Graphics	VME 32		VME 64	IBUS	GIO32	GIO32-bis	GIO64	EISA	PCI		XIO
		9U	6U	9U						1/2	Full	
Twin Tower12 Slot	All	8[1]										
Twin Tower15 Slot	All	4										
Diehard	All	4										
Predator	GTX, VGX, VGXT	6										
	Server	6 + 5[2]										
	SkyWriter	4										
Diehard2	Crimson	4										
Personal IRIS	All		1									
Eveready	Onyx - VTX, RE[2]			3	2 per IO4 board							
	Challenge L Server			5								
Terminator	Onyx - VTX, RE[2]			3 + 20 or 6[3]								
	Challenge XL Server			5 + 20[4]								
Indigo	R3000					2						
	R4000						2					
Indigo[2]	Extreme, XZ & XL							2[5]	4[5]			
	IMPACT							2[7]	3			
Indy	All						2					
O2	All									1		
OCTANE	All									1[8]	2[8]	4
Origin200	All										3	
Origin2000	Deskside, Rackmount									1[8]	2[8]	12
Onyx2	Deskside									1[8]	2[8]	6
	Rackmounts									1[8]	2[8]	12

4.10.1 VME32 (9U)

The VME32 slots can accept either 9U or 6U sized boards. 6U boards may be either installed directly into the backplane in P1 and P2 connectors, or can be installed on an extender.

Note that VME cards for SGI systems do not require front panels. Front panels are normally required for EMI sealing and connector mounting. Since all the system using VME (with the exception of the Personal IRIS) rely on the I/O Panel for EMI sealing, front panels are necessary. In fact, installing a 6U card with a front panel directly into the backplane will almost certainly cause the front panel to short out against any card in the slot to the right of the board.

Systems supporting VME32 have backplane pins that allow VSB connections to be made. VME64 slots do not.

4.10.1.1 Board Outline

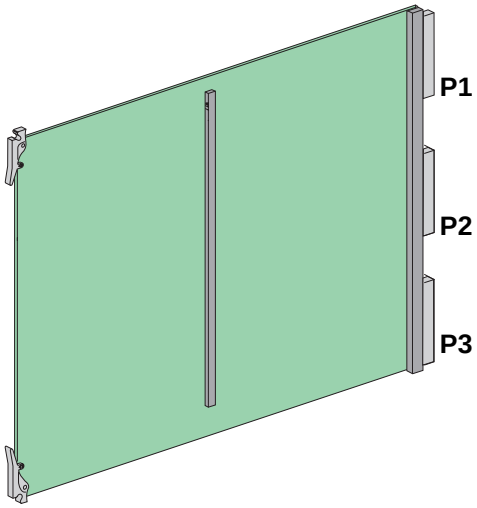

Figure 4-57 9U VME Board

4.10.1.2 Backplane Jumpering

VME backplanes require the four Bus Grant In & Out lines and the Interrupt Acknowledge line to be passed from one card slot to the next. On the early IRIS backplanes (specifically the 12 slot Twin Tower chassis) required jumpers to be put in place for these 5 signals for every empty slot to allow proper operation of the system. The 5 jumpers must removed for every slot where a board is installed.

Starting with the 15 Slot Twin Tower chassis, the backplanes were designed so that, in most cases, jumpers were not required. If VME cards were installed starting in the leftmost VME slot and with additional cards going into the next VME slot to the right, no jumpers would be required. If, however, an empty slot was left between two slots, or if the first VME card was not in the leftmost VME slot, jumpers would be required for each empty slot.

4.10.1.3 Power Budget

The table below shows the maximum current available for each of the supply voltages on the VME connectors.

Table 4-64 VME32 Power Budget (Twin & Single Towers)

Voltage	Max Current	Power
+ 5 V	5 A	25 W
+12 V	0.1 A	1.2 W
- 12 V	0.1 A	1.2 W
Total Power Budget (per slot)		**28 W**

An exception to this is that some DieHard chassis have one slot that complies with “Sun VME” power requirements. It’s power allocation is shown below:

Table 4-65 VME32 Power Budget (Diehard & Diehard2)

Voltage	Max Current	Power
+ 5 V	7 A	35 W
+12 V	0.1 A	1.2 W
- 12 V	0.1 A	1.2 W
-5.2 V	0.1 A	0.52 W
Total Power Budget (per slot)		**41 W**

4.10.1.4 Pinout

Table 4-66 VME32 Pinout

Pin	P1			P2			P3		
	A	B	C	A	B	C	A	B	C
1	D00	BBSY*	D08		+5V		+5V		GND
2	D01	BCLR*	D09		GND		+5V		GND
3	D02	ACFAIL	D10		RES.		+5V		GND
4	D03	BG0IN*	D11		A24		+5V		GND
5	D04	BG0OUT*	D12		A25		+5V		GND
6	D05	BG1IN*	D13		A26		+5V		GND
7	D06	BG1OUT*	D14		A27		+5V		GND
8	D07	BG2IN*	D15		A28		+5V		GND
9	GND	BG2OUT*	GND		A29		+5V		GND
10	SYSCLK	BG3IN*	SYSFAIL*		A30		+5V		GND
11	GND	BG3OUT*	BERR*	U	A31	U	+5V	U	GND
12	DS1*	BR0*	SYSRESET*	S	GND	S	+5V	S	GND
13	DS0*	BR1*	LWORD*		+5V		+5V		GND
14	WRITE*	BR2*	AM5	E	D16	E	+5V	E	GND
15	GND	BR3*	A23	R	D17	R	+5V	R	GND
16	DTACK	AM0	A22		D18		+5V		GND
17	GND	AM1	A21	D	D19	D	+5V	D	GND
18	AS*	AM2	A20	E	D20	E	+5V	E	GND
19	GND	AM3	A19	F	D21	F	+5V	F	GND
20	IACK*	GND	A18	I	D22	I	+5V	I	GND
21	IACKIN*	SERCLK	A17		D23		+5V		GND
22	IACKOUT*	SERDAT*	A16	N	GND	N	+5V	N	GND
23	AM4	GND	A15	E	D24	E	+5V	E	GND
24	A07	IRQ7*	A14	D	D25	D	+5V	D	GND
25	A06	IRQ6*	A13		D26		+5V		GND
26	A05	IRQ5*	A12		D27		+12V		+12V
27	A04	IRQ4*	A11		D28		+12V		+12V
28	A03	IRQ3*	A10		D29		-12V		-12V
29	A02	IRQ2*	A09		D30		-12V		-12V
30	A01	IRQ1*	A08		D31		Vee		Vee
31	-12V	+5STDBY	+12V		GND		Vee		Vee
32	+5V	+5V	+5V		+5V		Vee		Vee

4.10.2 VME32 (6U)

The Personal IRIS has one 6U sized VME slot. It's pinout is identical to the P1 and P2 pinouts described in Table 4-66, "VME32 Pinout", on page 4-116.

Access to the user defined pins of P2 is available in one of two different means depending on the Personal IRIS model. In the 4D/20 or 4D/25 access to the P2 user defined pins is only available inside the E-Module. A Eurocard style connector (AMP part number 650473-5) connects to the back of the VME slot P2 connector. This connection can, if necessary, be brought out of the E-Module via a blank panel just above the audio jacks on the I/O panel area.

On the 4D/30 and 4D/35, access to the user defined P2 pins are available via a high density 100 pin connector on the I/O panel area of the E-Module. This interface is documented in the next section.

For EMI purposes, VME boards must have an I/O Panel that provides a seal against the E-Module. The opening for the VME slot requires a panel different than the panels found on most "standard" VME boards (which, by their design do not provide any EMI sealing). A "standard" VME board will install into the single slot without any problem - but it will not provide any EMI sealing.

4.10.2.1 Board Outline

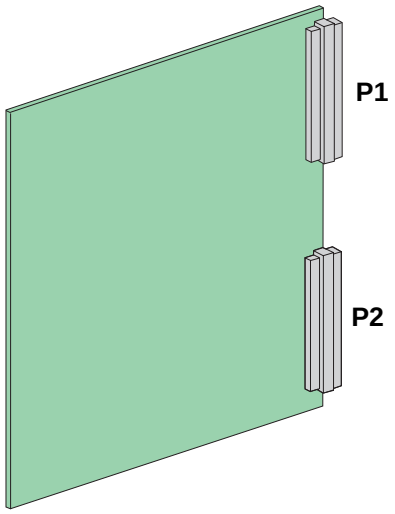

Figure 4-58 6U VME Board

4.10.2.2 Backplane Jumpering

Since there is only one slot in the Personal IRIS, there are no backplane jumpering considerations.

4.10.2.3 Power Budget

The table below shows the maximum current available for each of the supply voltages on the VME connectors.

Table 4-67 VME32 Power Budget (Personal IRIS)

Voltage	Max Current	Power
+ 5 V	5 A	25 W
+12 V	0.1 A	1.2 W
- 12 V	0.1 A	1.2 W
Total Power Budget (per slot)		**28 W**

4.10.3 VME P2 Expansion

Access to the user defined pins of the VME P2 connector is possible on most all of the IRIS systems that support VME. In the case of the Twin Tower, Diehard, Diehard2 and Eveready this is done by connecting to connector pins on the back of the backplane.

For the Personal IRIS two methods are used to connect to these pins. One, on the 4D/20 and 4D/25 is via a connection on the back of the P2 connector inside the E-Module. Using a Eurocard style connector will accomplish this.

On the 4D/30 and 4D/35 the user defined pins, as well as some power and ground connections are brought out to a high density 100 pin connector in the I/O Panel area of the E-Module. This section documents that interface.

4.10.3.1 Connector Drawing

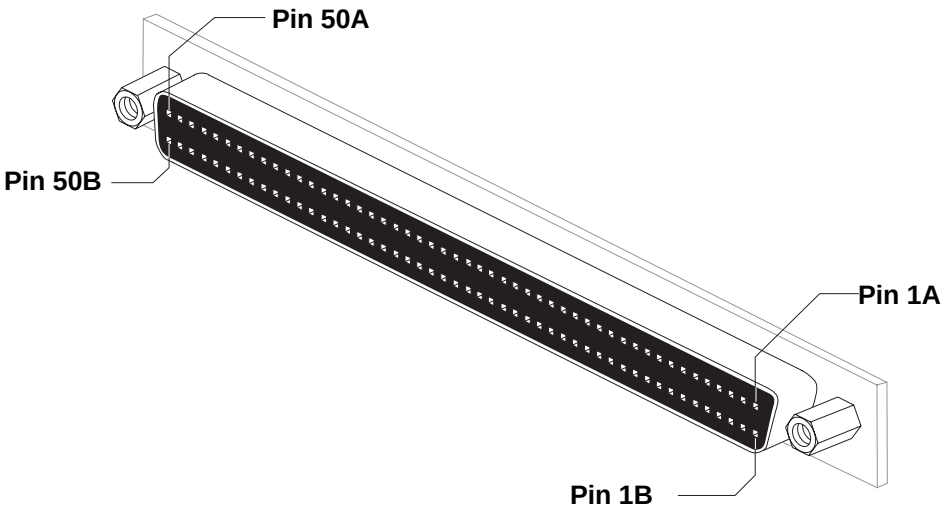

Figure 4-59 VME P2 Expansion Connector

4.10.3.2 Power Availability

The maximum current available at this connector for the voltages supplied is shown in the table below.

Table 4-68 VME P2 Expansion Power Budget

Voltage	Current	Power
+ 5 V	2.0 A	10 W
+12 V	2.0 A	24 W
- 12 V	2.0 A	24 W
Total Power Budget (per slot)		**58 W**

4.10.3.3 Pinout

Table 4-69 VME P2 Expansion Pinout (Personal IRIS)

Pin	SIgnal	Pin	Signal	Pin	Signal	Pin	Signal
1A	GND	1B	GND	26A	P2, A17	26B	P2, C17
2A	+5V	2B	+5V	27A	P2, A18	27B	P2, C18
3A	GND	3B	GND	28A	P2, A19	28B	P2, C19
4A	+5V	4B	+5V	29A	P2, A20	29B	P2, C20
5A	GND	5B	GND	30A	P2, A21	30B	P2, C21
6A	-12V	6B	-12V	31A	P2, A22	31B	P2, C22
7A	GND	7B	GND	32A	P2, A 23	32B	P2, C23
8A	-12V	8B	-12V	33A	P2, A 24	33B	P2, C24
9A	GND	9B	GND	34A	P2, A25	34B	P2, C25
10A	P2, A1	10B	P2, C1	35A	P2, A26	35B	P2, C26
11A	P2, A2	11B	P2, C2	36A	P2, A27	36B	P2, C27
12A	P2, A3	12B	P2, C3	37A	P2, A28	37B	P2, C28
13A	P2, A4	13B	P2, C4	38A	P2, A29	38B	P2, C29
14A	P2, A5	14B	P2, C5	39A	P2, A30	39B	P2, C30
15A	P2, A6	15B	P2, C6	40A	P2, A31	40B	P2, C31
16A	P2, A7	16B	P2, C7	41A	P2, A32	41B	P2, C32
17A	P2, A8	17B	P2, C8	42A	GND	42B	GND
18A	P2, A9	18B	P2, C9	43A	+5V	43B	+5V
19A	P2, A10	19B	P2, C10	44A	+5V	44B	+5V
20A	P2, A11	20B	P2, C11	45A	GND	45B	GND
21A	P2, A12	21B	P2, C12	46A	-12V	46B	-12V
22A	P2, A13	22B	P2, C13	47A	GND	47B	GND
23A	P2, A14	23B	P2, C14	48A	+12V	48B	+12V
24A	P2, A15	24B	P2, C15	49A	GND	49B	GND
25A	P2, A16	25B	P2, C16	50A	+12V	50B	+12V

4.10.4 VME64 (9U)

The VME64 slots available in the Onyx and Challenge systems are the same physical size as those found in other IRIS systems. However, they have additional data signals making the data bus 64 bits wide. These slots do not support VSB connections.

4.10.4.1 Board Outline

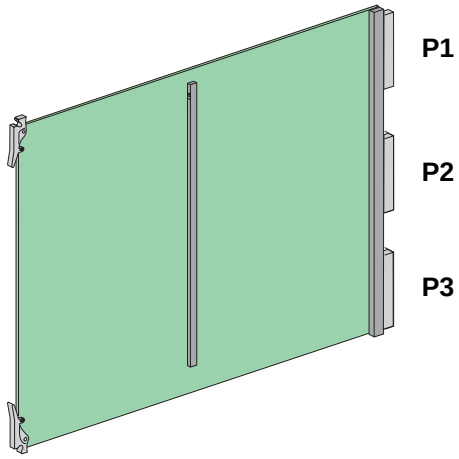

Figure 4-60 9U VME64 Board

4.10.4.2 Backplane Jumpering

Jumpering the Bus Grant In & Out and Interrupt Acknowledge signals follow the same rules as the VME slots in previous Single Tower and Rack systems.

In most cases, jumpers are not required. If VME cards are installed starting in the leftmost VME slot and with additional cards going into the next VME slot to the right, no jumpers would be required. If, however, an empty slot is left between two slots, or if the first VME card is not in the leftmost VME slot, jumpers are required for each empty slot.

4.10.4.3 Power Budget

Table 4-70 VME64 Power Budget (Onyx and Challenge)

Voltage	Current	Power
+ 5 V	8A	40 W
+12 V	0.2 A	2.4 W
- 12 V	0.2 A	2.4 W
-5.2 V	0.2 A	1 W
Total Power Budget (per slot)		**48 W**

4.10.4.4 Pinout

Table 4-71 VME64 Pinout

Pin	P1			P2			P3		
	A	B	C	A	B	C	A	B	C
1	D00	BBSY*	D08		+5V		+5V		GND
2	D01	BCLR*	D09		GND		+5V		GND
3	D02	ACFAIL	D10		RES.		+5V		GND
4	D03	BG0IN*	D11		A24		+5V		GND
5	D04	BG0OUT*	D12		A25		+5V		GND
6	D05	BG1IN*	D13		A26		+5V		GND
7	D06	BG1OUT*	D14		A27		+5V		GND
8	D07	BG2IN*	D15		A28		+5V		GND
9	GND	BG2OUT*	GND		A29		+5V		GND
10	SYSCLK	BG3IN*	SYSFAIL*		A30		+5V		GND
11	GND	BG3OUT*	BERR*	U	A31	U	+5V	U	GND
12	DS1*	BR0*	SYSRESET*	S	GND	S	+5V	S	GND
13	DS0*	BR1*	LWORD*		+5V		+5V		GND
14	WRITE*	BR2*	AM5	E	D16	E	+5V	E	GND
15	GND	BR3*	A23	R	D17	R	+5V	R	GND
16	DTACK*	AM0	A22		D18		+5V		GND
17	GND	AM1	A21	D	D19	D	+5V	D	GND
18	AS*	AM2	A20	E	D20	E	+5V	E	GND
19	GND	AM3	A19	F	D21	F	+5V	F	GND
20	IACK*	GND	A18		D22		+5V		GND
21	IACKIN*	SERCLK	A17	I	D23	I	+5V	I	GND
22	IACKOUT*	SERDAT*	A16	N	GND	N	+5V	N	GND
23	AM4	GND	A15	E	D24	E	+5V	E	GND
24	A07	IRQ7*	A14	D	D25	D	+5V	D	GND
25	A06	IRQ6*	A13		D26		+5V		GND
26	A05	IRQ5*	A12		D27		+12V		+12V
27	A04	IRQ4*	A11		D28		+12V		+12V
28	A03	IRQ3*	A10		D29		-12V		-12V
29	A02	IRQ2*	A09		D30		-12V		-12V
30	A01	IRQ1*	A08		D31		Vee		Vee
31	-12V	+5STDBY	+12V		GND		Vee		Vee
32	+5V	+5V	+5V		+5V		Vee		Vee

4.10.5 GIO32/32-bis

The GIO32 or GIO32-bis buses are used in the Indigo and Indy products (see Table 4-63, “Bus Interfaces on IRIS Systems”, on page 4-113 for specific details). Since the two GIO slots on these systems are both attached to the motherboard, or CPU board, it is possible to design a board that takes up both slot spaces.

GIO slots have a fixed address space. Slot 0 always occupies a particular address space while Slot 1 occupies a different address space. This is unlike VME where settings on the board itself determine the address the board responds to.

The I/O panels for Indigo and Indy are different. There is more space for connectors on the Indigo I/O panel. However, if a board is designed to fit the Indy I/O panel space, it will also fit in an Indigo - provided it has the appropriate I/O panel. This single wide board in the drawing below shows the Indy style I/O panel, while the double wide board shows the Indigo style I/O panel. Dimensions for both of these panels are available in the GIO Bus Specification.

4.10.5.1 Board Outline

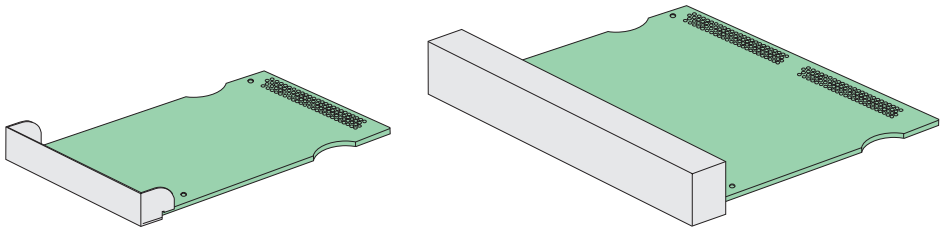

Figure 4-61 Single & Double GIO32/32-bis Boards

4.10.5.2 Power Budget

The following table shows the maximum current draw for voltages in a GIO slot.

Table 4-72 GIO32/32-bis Power Budget

Voltage	Current	Power
+ 5 V	2 A	10 W
+12 V	0.15 A	1.8 W
- 12 V	0.15 A	1.8 W
Total Power Budget (per slot)		**13.6 W**

4.10.5.3 Pinout

Consult the “GIO Bus Specification” for a complete pinout of the GIO32/32-bis bus.

4.10.6 GIO64 Bus

A GIO64 board is the same size as an EISA board. This is due to the fact that the two buses share four physical slots in the Indigo^2 (consult page 4-139 for a drawing and explanation).

The I/O panel space for a GIO64 board is identical to that for an EISA board.

4.10.6.1 Board Outline

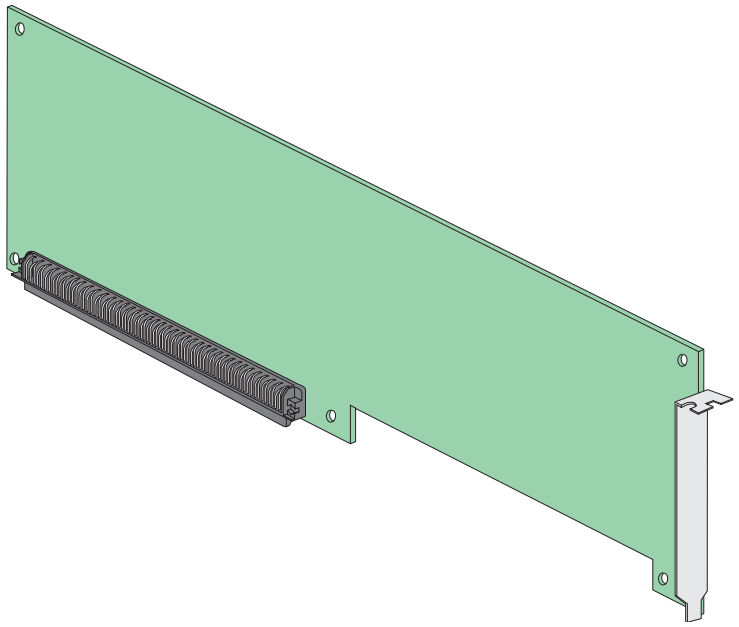

Figure 4-62 GIO64 Board

4.10.6.2 Power Budget

The following table shows the maximum current draw for voltages in a GIO64 slot.

Table 4-73 GIO64 Power Budget

Voltage	Current	Power
+ 5 V	4.5 A	22.5 W
+12 V	1 A	12 W
- 12 V	0.2 A	2.4 W
Total Power Budget (per slot)		**36.9 W**

4.10.6.3 Pinout

Consult the “GIO Bus Specification” for a complete pinout of the GIO64 bus.

4.10.7 EISA Bus

This is the same bus used by PC compatibles. EISA bus boards share four physical slots with GIO64 boards in the Indigo^2 (consult the section on backplanes for a drawing and explanation).

Since the EISA bus is a superset of the ISA bus, ISA boards will also fit into the Indigo^2.

An EISA or ISA board must have a software driver to integrate it with the IRIX operating system. This driver can be a user level driver or a kernel level driver. For more information about drivers in general, and EISA / ISA drivers specifically, consult the “IRIX Device Driver Programming Guide”.

4.10.7.1 Board Drawing

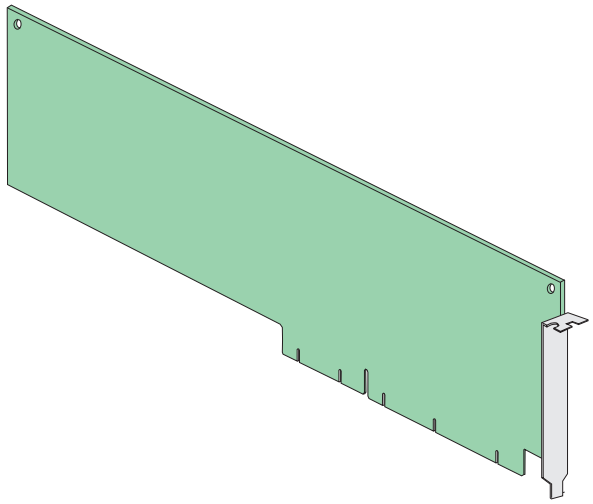

Figure 4-63 EISA Board

4.10.7.2 Power Budget

The following table shows the maximum current draw for voltages in an EISA slot.

Table 4-74 EISA / ISA Power Budget

Voltage	Current	Power
+ 5 V	4.5 A	22.5 W
- 5 V	0.1 A	0.5 W
+12 V	0.25 A	3.0W
- 12 V	0.08 A	1.0 W
Total Power Budget (per slot)		**27.0 W**

4.10.7.3 Pinout

Table 4-75 EISA / ISA Connector Pinout (Large Connector)

Row F	Row B	Pin	Row A	Row E
GND	GND	1	IOCHK*	CMD*
+5 V	RESET	2	SD7	START*
+5 V	+5 V	3	SD6	EXRDY
Reserved	IRQ9	4	SD5	EX32*
Reserved	-5 V	5	SD4	GND
Key	DRQ2	6	SD3	Key
Reserved	-12 V	7	SD2	EX16*
Reserved	SRDY*	8	SD1	SLBURST*
+12 V	+12 V	9	SD0	MSBURST*
M-IO	GND	10	IOCHRDY	W-R
LOCK	SMEMW*	11	AENx	GND
Reserved	SMEMR*	12	SA19	Reserved
GND	IOW*	13	SA18	Reserved
Reserved	IOR*	14	SA17	Reserved
BE3*	DACK3*	15	SA16	GND
Key	DRQ3	16	SA15	Key
BE2*	DACK1*	17	SA14	BE1*
BE0*	DRQ1	18	SA13	LA31*
GND	REFRESH*	19	SA12	GND
+5 V	BCLK	20	SA11	LA30*
LA29*	IRQ7	21	SA10	LA28*
GND	IRQ6	22	SA9	LA27*
LA26*	IRQ5	23	SA8	LA25*
LA24*	IRQ4	24	SA7	GND
Key	IRQ3	25	SA6	Key
LA16	DACK2*	26	SA5	LA15
LA14	TC	27	SA4	LA13
+5 V	BALE	28	SA3	LA12
+5 V	+5 V	29	SA2	LA11
GND	OSC	30	SA1	GND
LA10	GND	31	SA0	LA9
	Standard ISA Connections			
Extended ISA (EISA) Connections				

Table 4-76 EISA / ISA Connector Pinout (Small Connector)

Row H	Row D	Pin	Row C	Row G
LA8	MEMCS16*	1	SBHE*	LA7
LA6	IOCS16*	2	LA23	GND
LA5	IRQ10	3	LA22	LA4
+5 V	IRQ11	4	LA21	LA3
LA2	IRQ12	5	LA20	GND
Key	IRQ15	6	LA19	Key
DATA16	IRQ14	7	LA18	DATA17
DATA18	DACK0*	8	LA17	DATA19
GND	DRQ0	9	MEMR*	DATA20
DATA21	DACK5*	10	MEMW*	DATA22
DATA23	DRQ5	11	SD8	GND
DATA24	DACK6*	12	SD9	DATA25
GND	DRQ6	13	SD10	DATA26
DATA27	DACK7*	14	SD11	DATA28
Key	DRQ7	15	SD12	Key
DATA29	+5 V	16	SD13	GND
+5 V	MASTER16*	17	SD14	DATA30
+5 V	GND	18	SD15	DATA31
MAKx*		19		MREQx*
	Standard ISA Connections			
Extended ISA (EISA) Connections				

4.10.8 PCI Bus

The Silicon Graphics systems which support PCI bus cards comply with the PCI 2.1 revision of the PCI Specification. The boards are +5 Volt cards and the bus runs at 33 MHz. The systems will accept either 32 or 64 bit boards. The “PCI Developer Guide” covers the details of the PCI bus on Silicon Graphics systems. This document is available from the Developer Program.

As with other boards, a driver specific to the IRIX operating system is required to integrate a PCI board into a Silicon Graphics system. For information about writing device drivers for the IRIX operating system, consult the “IRIX Device Driver Programming Guide”. This document is available from Silicon Graphics Sales offices.

As shown in Table 4-63, there are both half size and full size PCI slots in the systems. These sizes comply with the sizes specified in the PCI Bus Specification. See the “Reference Information” in the Appendix.

4.10.8.1 Board Drawings

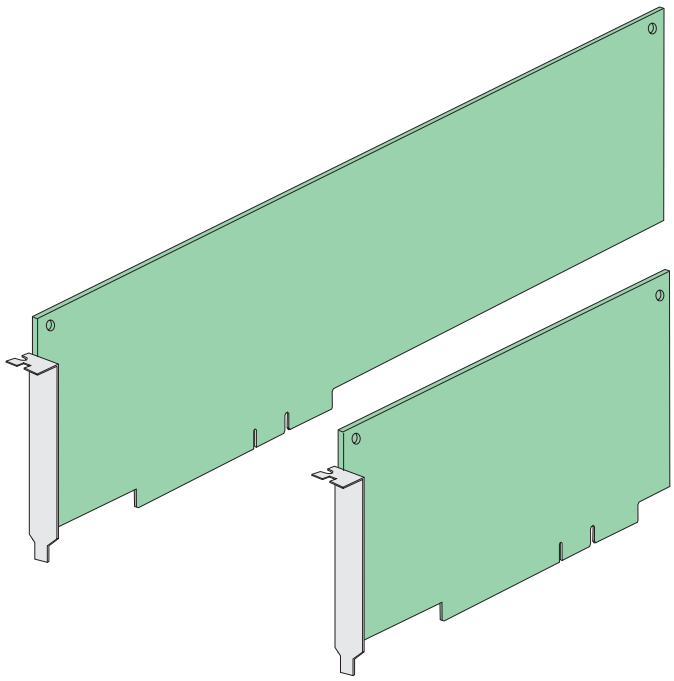

Figure 4-64 PCI Half-size and Full Size Boards

4.10.8.2 Power Budget

The available power for the systems that support PCI is shown in table below.

The O2, with its one half-size PCI slot has less power available than the other systems that support PCI. The O2 is a 5 Volt only environment - if 3.3 Volts is required on the board, it must be generated by an on-board regulator from either the 5 Volt of 12 Volt supply lines.

For OCTANE's three slots there is a total of 45 Watts of 5 Volt power available. There is also 3.3 Volts available on the bus. From Table 4-77, it is possible to exceed the total power budget for all slots by combining the 5 Volt power and 3.3 Volt power. This is not allowed. A card may not use more than 15 Watts of combined power from either 5 Volts or 3.3 Volts.

The Origin200, Origin2000 and Onyx2 are similar to the OCTANE in that the total power from both 5 Volt and 3.3 Volt sources may not exceed the per slot power budget.

Table 4-77 PCI Power Budget

System	Total Watts		Current Available (per slot)	
	All Slots	Per Slot	5 Volts	3.3 Volts
O2	10 W	10 W	2.0 Amps	
OCTANE	45 W	15 W	3.0 Amps	3.3 Amps
Origin200	75 W	25 W	5.0 Amps	3.3 Amps
Origin2000	75 W	25 W	5.0 Amps	2.2 Amps
Onyx2	75 W	25 W	5.0 Amps	2.2 Amps

4.10.8.3 Connector Pinout

Table 4-78 shows the pinout for the PCI connector used on Silicon Graphics systems. The pins shown in the shaded area of the table are those required only for 64 bit PCI cards.

Table 4-78 PCI Connector Pinout

Pin	Signal Name	Description
A1	TRST	Test Logic Reset
A2	+12V	+12 VDC
A3	TMS	Test Mde Select
A4	TDI	Test Data Input
A5	+5V	+5 VDC
A6	INTA	Interrupt A
A7	INTC	Interrupt C
A8	+5V	+5 VDC
A9	RESV01	Reserved VDC
A10	+5V	+V I/O
A11	RESV03	Reserved VDC
A12	GND03	Ground or Open (Key)
A13	GND05	Ground or Open (Key)
A14	RESV05	Reserved VDC
A15	RESET	Reset
A16	+5V	+V I/O
A17	GNT	Grant PCI use
A18	GND08	Ground
A19	RESV06	Reserved VDC
A20	AD30	Address/Data 30
A21	+3.3V01	+3.3 VDC
A22	AD28	Address/Data 28
A23	AD26	Address/Data 26
A24	GND10	Ground
A25	AD24	Address/Data 24
A26	IDSEL	Initialization Device Select
A27	+3.3V03	+3.3 VDC
A28	AD22	Address/Data 22
A29	AD20	Address/Data 20
A30	GND12	Ground
A31	AD18	Address/Data 18
A32	AD16	Address/Data 16
A33	+3.3V05	+3.3 VDC
A34	FRAME	Address or Data phase
A35	GND14	Ground
A36	TRDY	Target Ready
A37	GND15	Ground
A38	STOP	Stop Transfer Cycle
A39	+3.3V07	+3.3 VDC
A40	SDONE	Snoop Done
A41	SBO	Snoop Backoff
A42	GND17	Ground
A43	PAR	Parity
A44	AD15	Address/Data 15
A45	+3.3V10	+3.3 VDC
A46	AD13	Address/Data 13
A47	AD11	Address/Data 11
A48	GND19	Ground
A49	AD9	Address/Data 9
A50	(OPEN)	Ground or Open (Key)

Pin	Signal Name	Description
B1	-12V	-12 VDC
B2	TCK	Test Clock
B3	GND	Ground
B4	TDO	Test Data Output
B5	+5V	+5 VDC
B6	+5V	+5 VDC
B7	INTB	Interrupt B
B8	INTD	Interrupt D
B9	PRSNT1	Reserved
B10	RES	+V I/O
B11	PRSNT1	Present
B12	GND	Ground or Open (Key)
B13	GND	Ground or Open (Key)
B14	RES	Reserved VDC
B15	GND	Reset
B16	CLK	Clock
B17	GND	Ground
B18	REQ	Request
B19	+5V	+V I/O
B20	AD31	Address/Data 31
B21	AD29	Address/Data 29
B22	GND	Ground
B23	AD27	Address/Data 27
B24	AD25	Address/Data 25
B25	+3.3V	+3.3VDC
B26	C/BE3	Command, Byte Enable 3
B27	AD23	Address/Data 23
B28	GND	Ground
B29	AD21	Address/Data 21
B30	AD19	Address/Data 19
B31	+3.3V	+3.3 VDC
B32	AD17	Address/Data 17
B33	C/BE2	Command, Byte Enable 2
B34	GND13	Ground
B35	IRDY	Initiator Ready
B36	+3.3V06	+3.3 VDC
B37	DEVSEL	Device Select
B38	GND16	Ground
B39	LOCK	Lock bus
B40	PERR	Parity Error
B41	+3.3V08	+3.3 VDC
B42	SERR	System Error
B43	+3.3V09	+3.3 VDC
B44	C/BE1	Command, Byte Enable 1
B45	AD14	Address/Data 14
B46	GND18	Ground
B47	AD12	Address/Data 12
B48	AD10	Address/Data 10
B49	GND20	Ground
B50	(OPEN)	Ground or Open (Key)

Table 4-78 PCI Connector Pinout

Pin	Signal Name	Description
A51	(OPEN)	Ground or Open (Key)
A52	C/BE0	Command, Byte Enable 0
A53	+3.3V11	+3.3 VDC
A54	AD6	Address/Data 6
A55	AD4	Address/Data 4
A56	GND21	Ground
A57	AD2	Address/Data 2
A58	AD0	Address/Data 0
A59	+5V	+V I/O
A60	REQ64	Request 64 bit
A61	VCC11	+5 VDC
A62	VCC13	+5 VDC
A63	GND	Ground
A64	C/BE[7]#	Command, Byte Enable 7
A65	C/BE[5]#	Command, Byte Enable 5
A66	+5V	+V I/O
A67	PAR64	Parity 64
A68	AD62	Address/Data 62
A69	GND	Ground
A70	AD60	Address/Data 60
A71	AD58	Address/Data 58
A72	GND	Ground
A73	AD56	Address/Data 56
A74	AD54	Address/Data 54
A75	+5V	+V I/O
A76	AD52	Address/Data 52
A77	AD50	Address/Data 50
A78	GND	Ground
A79	AD48	Address/Data 48
A80	AD46	Address/Data 46
A81	GND	Ground
A82	AD44	Address/Data 44
A83	AD42	Address/Data 42
A84	+5V	+V I/O
A85	AD40	Address/Data 40
A86	AD38	Address/Data 38
A87	GND	Ground
A88	AD36	Address/Data 36
A89	AD34	Address/Data 34
A90	GND	Ground
A91	AD32	Address/Data 32
A92	RES	Reserved
A93	GND	Ground
A94	RES	Reserved

Pin	Signal Name	Description
B51	(OPEN)	Ground or Open (Key)
B52	AD8	Address/Data 8
B53	AD7	Address/Data 7
B54	+3.3V12	+3.3 VDC
B55	AD5	Address/Data 5
B56	AD3	Address/Data 3
B57	GND22	Ground
B58	AD1	Address/Data 1
B59	VCC08	+5 VDC
B60	ACK64	Acknowledge 64 bit
B61	VCC10	+5 VDC
B62	VCC12	+5 VDC
B63	RES	Reserved
B64	GND	Ground
B65	C/BE[6]#	Command, Byte Enable 6
B66	C/BE[4]#	Command, Byte Enable 4
B67	GND	Ground
B68	AD63	Address/Data 63
B69	AD61	Address/Data 61
B70	+5V	+V I/O
B71	AD59	Address/Data 59
B72	AD57	Address/Data 57
B73	GND	Ground
B74	AD55	Address/Data 55
B75	AD53	Address/Data 53
B76	GND	Ground
B77	AD51	Address/Data 51
B78	AD49	Address/Data 49
B79	+5V	+V I/O
B80	AD47	Address/Data 47
B81	AD45	Address/Data 45
B82	GND	Ground
B83	AD43	Address/Data 43
B84	AD41	Address/Data 41
B85	GND	Ground
B86	AD39	Address/Data 39
B87	AD37	Address/Data 37
B88	+5V	+V I/O
B89	AD35	Address/Data 35
B90	AD33	Address/Data 33
B91	GND	Ground
B92	RES	Reserved
B93	RES	Reserved
B94	GND	Ground

4.10.9 XIO Bus

The XIO bus is a very high speed bus implemented in the most recent systems. The XIO boards can be single slot, double slot, or may be double wide - like the IO6 BaseIO boards for the Origin2000 and Onyx2. The optional PCI card cages that are available for OCTANE, Origin2000 and Onyx2 are really XIO boards that take one of the wide XIO slots.

The XIO modules for Origin2000 and Onyx2 differ from the XIO modules for the OCTANE in the latching mechanisms they use. Also, the location of the latching mechanism will determine in which slots a particular board can be installed. An example of this is the module in Figure 4-65 that has a latch lever on the bottom of the module, not the top.

Figure 4-65 shows an example of each of these types of boards.

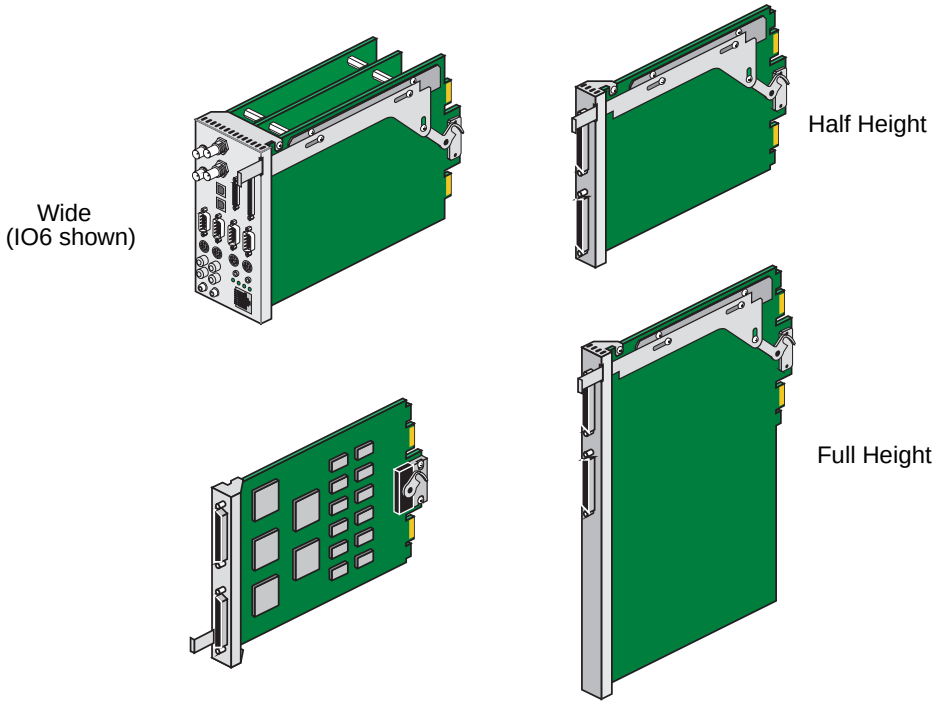

Figure 4-65 XIO Boards