4.9 CPU Interfaces

Starting with the Onyx and Challenge machines Interrupt Inputs and Outputs have been available on the high end systems. These interfaces can be used to synchronize two or more machines. Table 4-60 shows the systems where these interfaces are available.

Table 4-60 CPU Interrupt Interfaces

Chassis	CPU Input(s)	CPU Output(s)
Onyx	2	4
Challenge L & XL	2	4
Origin 2000	1	1
Onyx2	1	1

4.9.1 3 Conductor Audio Jack and Plug

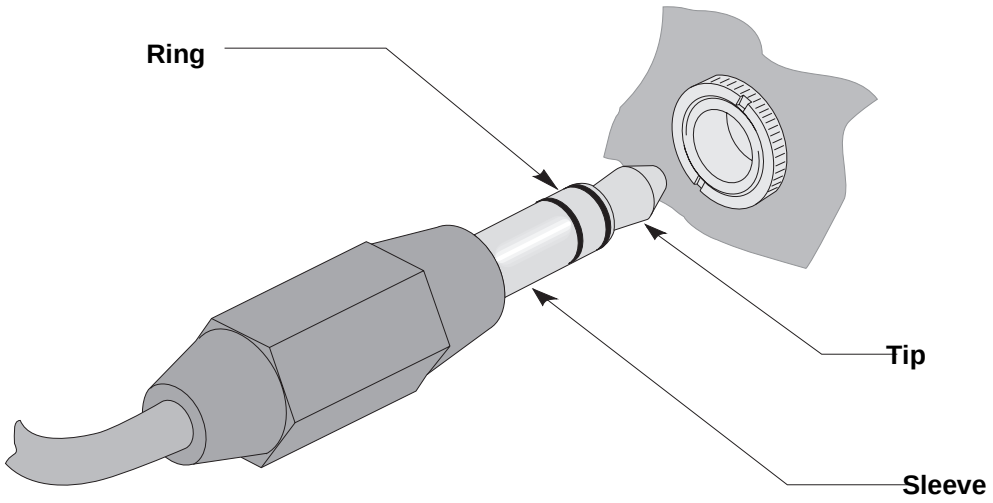

Figure 4-56 Interrupt Jack and Plug

4.9.2 Pinout

Table 4-61 Interrupt Input/Output Pinout

Pin	Signal
Tip	Interrupt Input/Output (active low)
Ring	+5 Volts
Sleeve	Chassis Ground/ Cable Shield

4.9.3 Interrupt Inputs

These inputs allow an interrupt signal generated by another machine to directly control the system. For example, a particular action in software could be programmed to wait for the receipt of an interrupt signal from another machine.

These inputs are opto-isolated and operate as an open collector current loop. The source resistance is 420 ohms pulled up to +5 Volts. The connections are via a 3 conductor 1/8" audio jack. The connector pinouts are shown in Table 4-61.

On those systems with more than one interrupt input the system does not distinguish between a signal received at either of the two input connections. Therefore it is unimportant which connector is used for an input interrupt. For more information on this signal consult the 'ei' (external interrupt) manpage.

4.9.4 Interrupt Outputs

There are four interrupt outputs. The interrupt outputs are used to send an interrupt signal to another machine for synchronization purposes. Some systems have one interrupt output, others have four outputs (see Table 4-60). Unlike the Interrupt Inputs, the outputs can be individually driven.

Like the inputs, the outputs are opto-isolated and operate as an open collector current loop. The source resistance is 420 ohms pulled up to +5 Volts. The connections are via a 3 conductor 1/8" audio jack. The connector pinouts are shown in Table 4-61.

For more information on this signal consult the 'ei' (external interrupt) manpage.